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(71) Applicant:
Hewlett-Packard Company
Palo Alto, California 94304 (US)

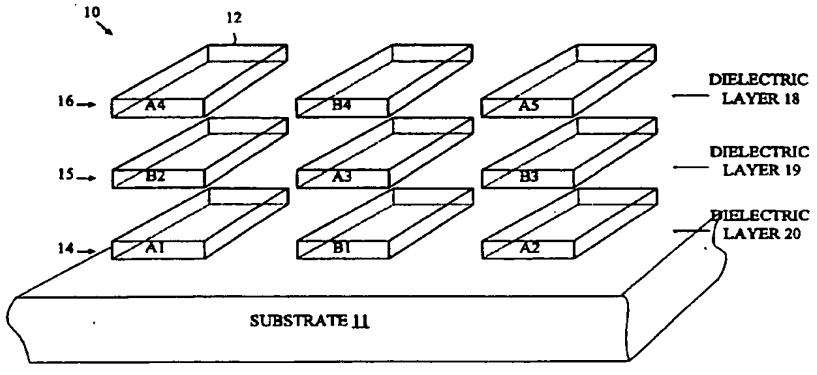
(72) Inventors:
- **Nishimura, Ken A.**
  Mountain View, CA 94040 (US)
- **Willingham, Scott D.**
  Sunnyvale, CA 94087 (US)
- **McFarland, William J.**
  Redwood City, CA 94061 (US)

(74) Representative:
Liesegang, Roland, Dr.-Ing.
FORRESTER & BOEHMERT
Franz-Joseph-Strasse 38
80801 München (DE)

(54) Stacked-fringe integrated circuit capacitors

(57) A capacitor[10, 50, 100] that is adapted for construction over a substrate[11] in the metal interconnect layers provided by conventional integrated circuit processes. The capacitor[10, 50, 100] includes a first conducting layer[14, 102] separated from the substrate[11] by a first dielectric layer[20] and a second conducting layer[15, 102] separated from the first conduction layer by a second dielectric layer[19]. The second conducting layer[15, 102] is divided into a plurality of electrically isolated conductors in an ordered array. Every other one of the conductors is connected to a first terminal[31], and the remaining conductors are connected to a second terminal[32]. The first conducting layer[14, 102] includes at least one conductor which is connected to the first terminal[31]. In one embodiment of the invention, the first conducting layer[14, 102] also includes a plurality of electrically isolated conductors in an ordered array, every other one of the conductors being connected to the first terminal[31] and the remaining conductors being connected the second terminal[32].

FIGURE 1



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Descripti n

Field of the Invention

[0001] The present invention relates to integrated circuits, and more particularly, to capacitors for use in integrated circuits.

Background of the Invention

[0002] Analog integrated circuits must rely primarily on capacitors to provide reactances, since traditional IC processes do not allow the fabrication of inductances. The limitations imposed by conventional IC processes on capacitors restrict the type of circuits that can be realized using these processes.

[0003] Traditional analog IC processes construct capacitors by sandwiching a dielectric layer between conductors. For example, a polysilicon layer deposited over the silicon substrate can serve as conductors with a thin oxide dielectric. Gate oxide layers are very thin, and hence this type of structure has a very high specific capacitance. Unfortunately, the polysilicon layers and terminals deposited thereon form a MOS structure which leads to a highly non-linear capacitor unless a large DC bias is maintained across the capacitor. Such biases are incompatible with the low power supply voltages used with modern circuits. Further, MOS capacitors are polarized, and hence, cannot be used in circuits such as switched-capacitor circuits in which the terminals of the capacitor are flipped in polarity.

[0004] Capacitors may also be constructed using the metal interconnect layers with a dielectric layer between the metal layers to form a metal-metal capacitor. While such capacitors avoid the problems discussed above with respect to MOS capacitors, metal-metal capacitors have two drawbacks of their own. The interlayer dielectrics are relatively thick; hence, metal-metal capacitors have relatively low specific capacitances. Second, such capacitors suffer from parasitic, or "back-plate" capacitance between one, or both, of the terminals and the substrate of the IC. In most processes, the dielectric thickness between the interconnect layers is roughly equal to the dielectric thickness between the substrate and the bottom interconnect layer. Hence, the parasitic capacitance is roughly equal to the active capacitance.

[0005] IC processes having a third layer of metal interconnect have become common. In such processes, a stacked plate structure can be used to provide an improved capacitor structure over the metal-metal structure described above. In this case, the capacitor has two dielectric layers sandwiched between the three metal layers. The outer metal layers are electrically connected to form one terminal of the capacitor, while the middle layer forms the other terminal. This doubles the specific capacitance while leaving the parasitic capacitance approximately the same. Hence, such structures have roughly a 2:1 active to parasitic capacitance ratio. While this represents an improvement over the two layer capacitor construction, there is still a need for an improved capacitor structure.

[0006] Broadly, it is the object of the present invention to provide a improved integrated capacitor structure.

[0007] It is a further object of the present invention to provide a capacitor structure that has higher active capacitances than obtainable with prior art metal-metal processes.

[0008] It is a still further object of the present invention to provide a capacitor structure that has reduced parasitic capacitance on one of its terminals.

[0009] These and other objects of the present invention will become apparent to those skilled in the art from the following detailed description of the invention and the accompanying drawings.

Summary of the Invention

[0010] The present invention is a capacitor that is adapted for construction over a substrate in the metal interconnect layers provided by conventional integrated circuit processes. The capacitor includes a first conducting layer separated from the substrate by a first dielectric layer and a second conducting layer separated from the first conducting layer by a second dielectric layer. The second conducting layer is divided into a plurality of electrically isolated conductors in an ordered array. Every other one of the conductors is connected to a first terminal, and the remaining conductors are connected to a second terminal. The first conducting layer includes at least one conductor which is connected to the first terminal. In one embodiment of the invention, the first conducting layer also includes a plurality of electrically isolated conductors in an ordered array, every other one of the conductors being connected to the first terminal and the remaining conductors being connected the second terminal.

Brief Description of the Drawings

[0011]

Figure 1 is a perspective view of the conductors in a capacitor according to the present invention.

Figure 2 is a top view of the capacitor shown in Figure 1.

Figure 3 is a cross-sectional view of the capacitor shown in Figure 1.

Figure 4 is a schematic diagram of the equivalent electrical circuit for a capacitor according to the present invention.

Figure 5 is a perspective view of the conductors in another embodiment of a capacitor according to the

present invention.

Figure 6 is a perspective view f the conductors in a third embodiment of a capacitor according to the present invention.

Detailed Description of the Invention

[0012] The manner in which the present invention obtains its advantages may be more easily understood with reference to Figure 1 which is a perspective view of the conductors 12 in a capacitor 10 according to the present invention constructed in a three metal layer process deposited over a substrate 11. The conductors in the first metal layer are shown at 14, those in the second metal layer are shown at 15, and those in the top metal layer are shown at 16. The space between substrate 11 and metal layer 14 is assumed to be filled with a dielectric layer 20. The conductors are connected such that all of the "A" conductors are connected together, and all of the "B" conductors are connected together. To simplify this drawing, the interconnects between the "A" conductors and "B" conductors have been omitted. In addition, the dielectric layers 18 and 19 which fill the space between the metal layers and metal lines in each layer has also been omitted from the drawing.

[0013] The interconnections between the A and B conductors may be more easily understood with reference to Figures 2 and 3. Figure 2 is a top view of capacitor 10, and Figure 3 is cross-sectional view of capacitor 10 through line 21-22. The A conductors are offset from the B conductors such that the conductors in the various layers of the same type may be connected together with the aid of a vertical via. The vias are shown in phantom in Figure 2. Typical vias are shown at 23 and 24. The A conductors are connected to a first terminal 31, denoted by "terminal A", and the B conductors are connected to a second terminal 32 denoted by "terminal B".

[0014] The capacitance between the "A" and "B" conductors results from the conventional parallel plate capacitance between conductors in different levels of metal interconnect and the fringe capacitance between conductors in the same layer of metal. The "A" and "B" conductors are arranged such that each "A" conductor is surrounded by "B" conductors and vice versa within the body of the capacitor. The relative dimensions of metal line width and thickness, and dielectric separation obtained with modern IC processes result in large fringe fields such as between conductors B2 and A3. This fringe capacitance more than overcomes the loss in parallel-plate capacitance due to the gaps in the metal when compared to an equivalent area flat-plate structure.

[0015] It is advantageous to minimize the parasitic capacitance between the "A" conductors and substrate 11 and between "B" conductors and substrate 11. Conventional flat-plate capacitors present a parasitic capacitance from the lower metal plate to th substrate due to the parallel-plate capacitanc between the substrate and the bottom plate. The embodiment shown in Figure 1 has a reduced parasitic capacitance because of the gaps between the metal conductors which reduce the plate area of the bottom plate of the parasitic capacitor. In addition, the alternating connection of the metal lines at the lowest level results in the parasitic capacitance being divided equally between the A and B terminals of the capacitor. Finally, the fringing capacitance generated by the edges of the metal lines to the substrate is reduced by the alternating conductor configuration since the B conductors partially shield the A conductors in the bottom layer.

[0016] While the example shown in Figure 1 has only three columns of metal conductors, it is to be understood that the structure can be extended horizontally over the substrate by adding metal conductors to form a structure that is three conductors high and an arbitrary number of conductors wide.

[0017] The improvement provided by the present invention may be seen by comparing the capacitance of a conventional stacked plate capacitor constructed from three metal plates 100mm x 100mm, with a capacitor according to the present invention in which each of the plates is divided into conductors to form 42 metal lines having a length of 100mm. The equivalent circuit of both of the capacitors is shown in Figure 4. The capacitance between the A and B terminals of the capacitor is denoted by C_{AB}. The parasitic capacitance between the A terminal and the substrate is denoted by C_A. The parasitic capacitance between the B terminal and the substrate is denoted by C_B. For the conventional capacitor, C_{AB} was found to be 750 fF, compared to 1220 fF for the present invention. Hence, the present invention provides higher specific capacitance than the conventional structure. The present invention also provides reduced parasitic capacitance. For the conventional capacitor, C_A and C_B were 280 fF and 5fF respectively. For the present invention, these values were both 120fF. Hence, the present invention also provides reduced parasitic capacitance.

[0018] In some circumstances, the presence of a parasitic capacitance on one of the terminals of a capacitor is unacceptable. For such cases, the embodiment of the present invention shown in Figure 1 can be modified by removing the metal lines on the bottom layer corresponding to the terminal in question. For example, all of the B conductors in layer 14 could be eliminated as shown in Figure 5, which is a prospective view of a capacitor 50 according to the present invention. While this results in a loss of active capacitance, virtually all of the capacitance between terminal B and the substrate is eliminated. In the example discussed above, the removal of all of the B conductors resulted in a drop in C_{AB} from 1220fF to 907fF with C_A=197fF and C_B =7.5fF. It should be noted that even with this reduction in active capacitance, the present invention provides significantly

more active capacitance and significantly less parasitic capacitance than the conventional stacked plate capacitor.

[0019] The above described embodiments of the present invention have utilized a rectangular array of metal strips in which the strips were all parallel to one another. However, embodiments in which the strips are not parallel may also be constructed. Refer now to Figure 6 which is a perspective view of a capacitor 100 according to the present invention which has been constructed over a substrate 111 utilizing a 3 layer metal process. The strips constructed in the first metal layer are shown at 101; a typical strip is shown at 114. The strips constructed in the second metal layer are shown at 102; a typical strip is shown at 113. Finally, the strips constructed in the third metal layer are shown at 103; a typical strip is shown at 112. It will be noted that the strips constructed in the second layer are at right angles to those constructed in the first and third metal layers. The strips are connected such that all of the "A" conductors are connected together, and all of the "B" conductors are connected together. The strips in each layer are arranged such that the conductors alternate between "A" and "B" conductors.

[0020] The above described embodiments of the present invention utilized three layers of conductors because currently available fabrication processes provide three layers of metal interconnect. However, it will be apparent to those skilled in the art from the foregoing discussion that the minimum number of layers is two and that additional layers may be utilized if the integrated circuit processing scheme permits more layers of metal interconnect.

[0021] While the above described embodiments of the present invention have utilized metallic strips in each of the metal layers, it will be apparent to those skilled in the art from the above discussion that other shapes may be utilized. Strips are preferred because of the ease of patterning the strips using conventional lithographic techniques. However, increased capacitance from the fringing field between adjacent conductors in each layer may be obtained by using more complex shapes that provide increased surface area between the adjacent conductors.

[0022] Various modifications to the present invention will become apparent to those skilled in the art from the foregoing description and accompanying drawings. Accordingly, the present invention is to be limited solely by the scope of the following claims.

Claims

1. A capacitor[10, 50, 100] constructed over a substrate[11], said capacitor[10, 50, 100] comprising:

   a first conducting layer[14, 102] separated from said substrate[11] by a first dielectric layer[20]; and

   a second conducting layer[15, 102] separated from said first conduction layer by a second dielectric layer[19];

   wherein said second conducting layer[15, 102] is divided into a plurality of electrically isolated conductors[12, 112] in an ordered array, every other one of said conductors being connected to a first terminal[31] and the remaining conductors being connected to a second terminal[32], and wherein said first conducting layer[14, 102] includes at least one conductor which is connected to said first terminal[31].

2. The capacitor[10, 50, 100] of Claim 1 wherein said first conducting layer[14, 102] comprises a plurality of electrically isolated conductors in an ordered array, every other one of said conductors being connected to said first terminal[31] and the remaining conductors being connected to said second terminal[32].

3. The capacitor[10, 50, 100] of Claim 1 wherein none of said conductors in said first conducting layer[14, 102]s is connected to said second terminal[32].

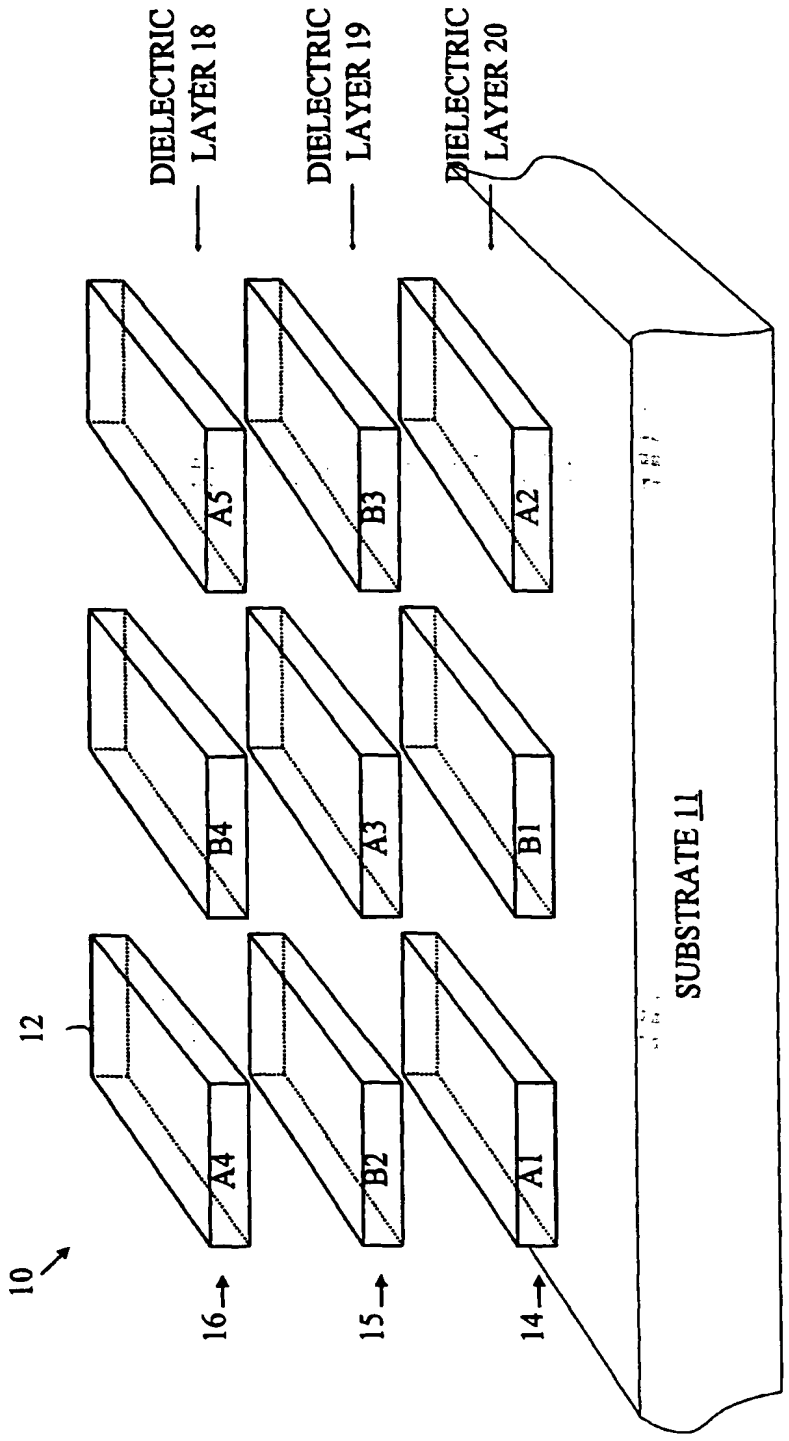
4. The capacitor[10, 50, 100] of Claim 1 wherein said conductors comprise rectangular metallic strips.

5. The capacitor[10, 50, 100] of Claim 4 wherein said metallic strips in said first metallic layer[14] are parallel to said metallic strips in said second metallic layer[151].

6. The capacitor[10, 50, 100] of Claim 4 wherein said metallic strips in said first metallic layer[101] are perpendicular to said metallic strips in said second metallic layer[102].

7. The capacitor[10, 50, 100] of Claim 2 wherein the conductors in said second metallic layer that are connected to said first terminal[31] are chosen so as to maximize the capacitance between said first and second terminals.

FIGURE 1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DIELECTRIC LAYER 19
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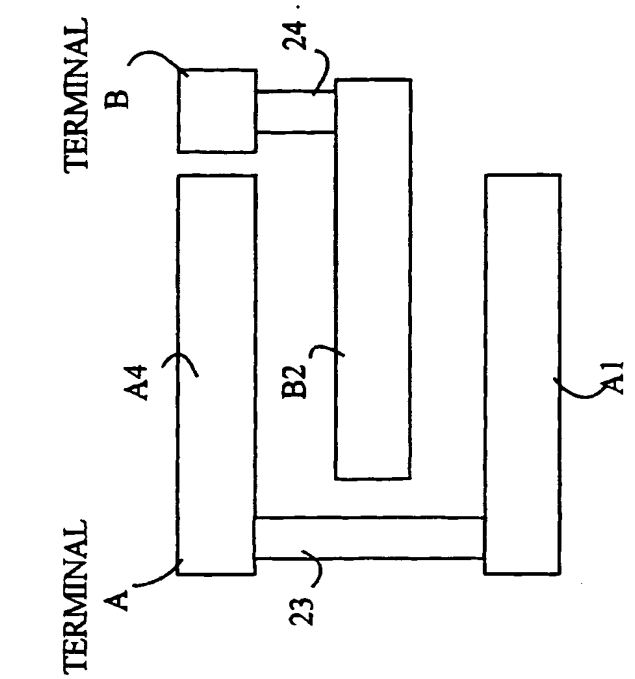


FIGURE 3

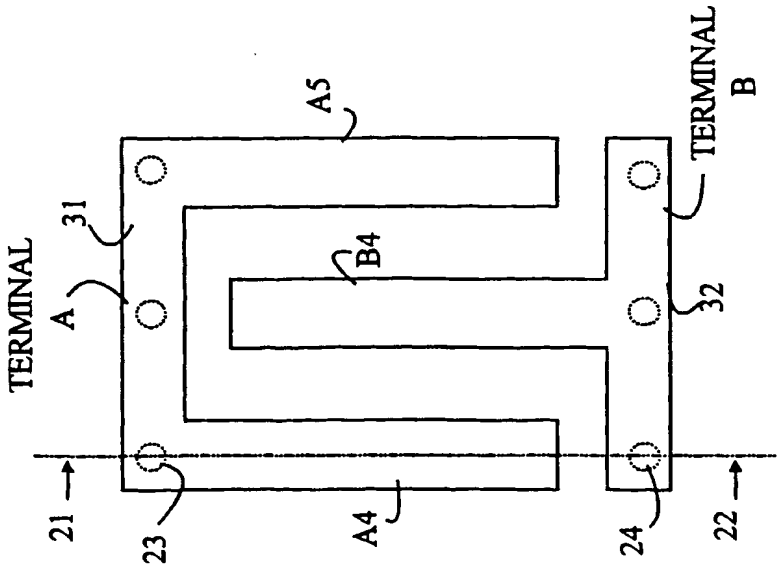


FIGURE 2

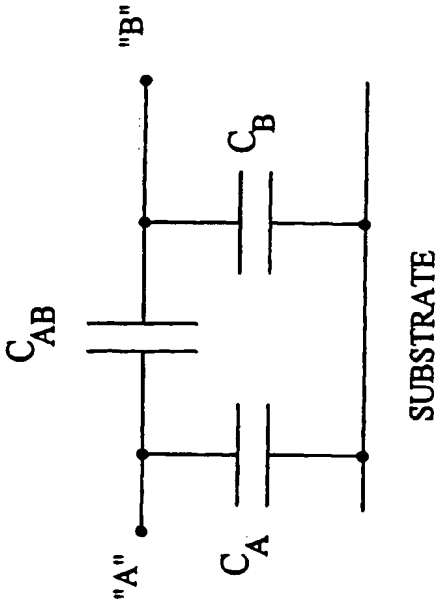
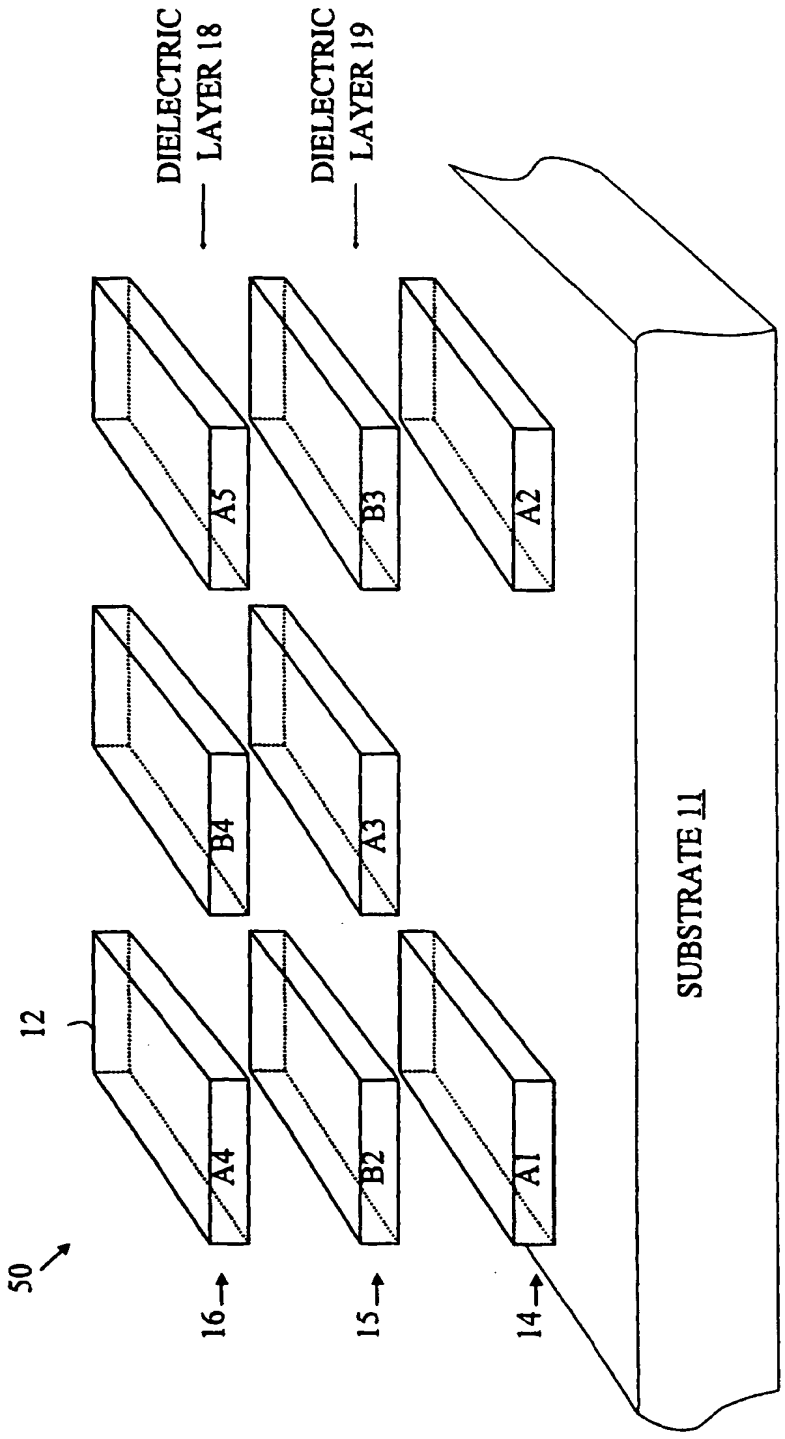


FIGURE 4

FIGURE 5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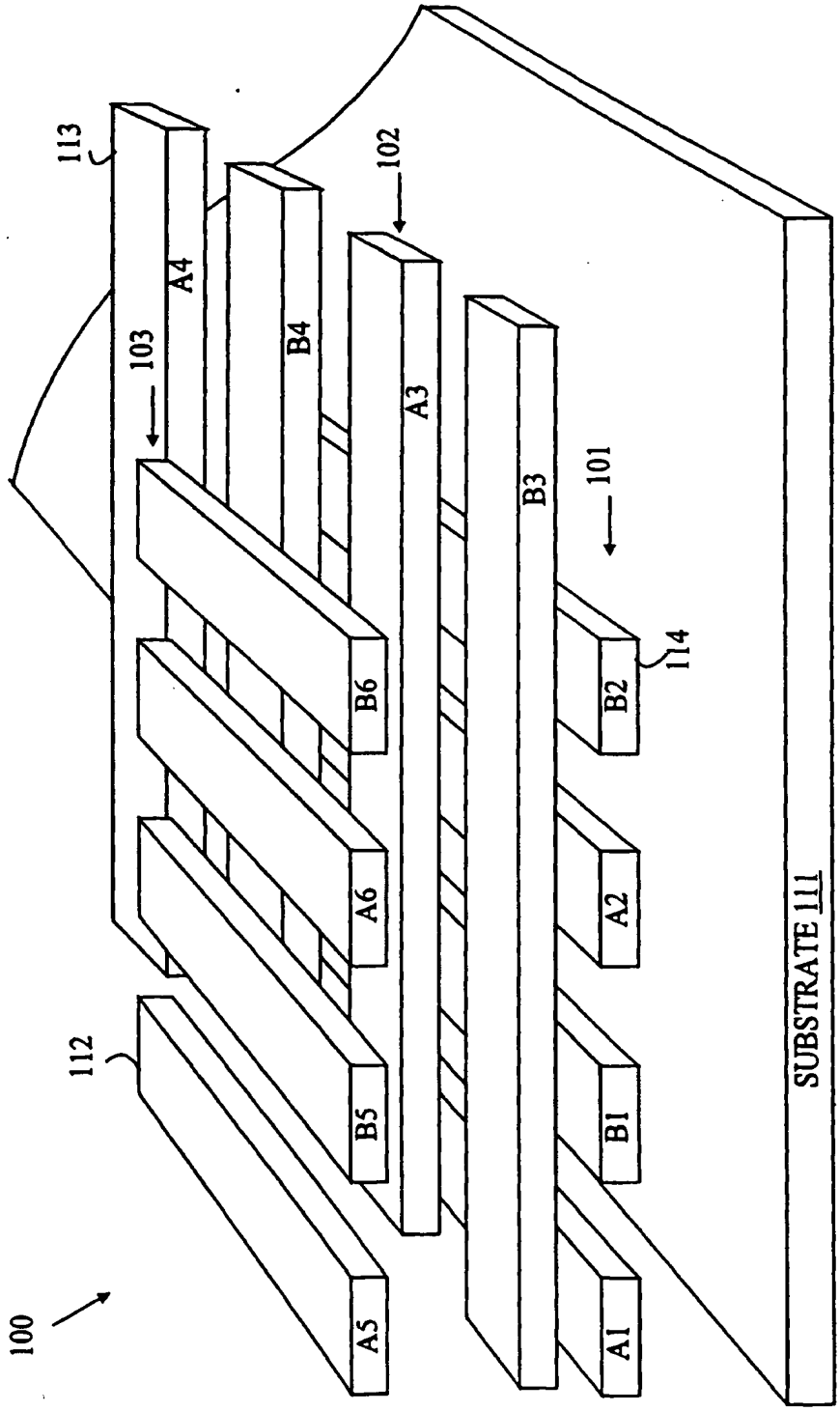
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FIGURE 6